COLOR SEPARATOR CIRCUIT AND CHROMINANCE SIGNAL PROCESSING DEVICE PROVIDED THEREWITH

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a color separator circuit for separating colors to reproduce chrominance signals from image signals and to a chrominance signal processing device provided with such a color separator circuit. The present invention relates particularly to a color separator circuit that performs color separation on image signals output from a solid-state image-sensing device and to a chrominance signal processing device provided with such a color separator circuit.

Description of the Prior Art

[0002] When chrominance signals are produced from image signals output from a solid-state image-sensing device, such as a single-panel color CCD (charge-coupled device) or a two-panel color CCD, that is provided with a plurality of types of color filters, from the image signals obtained for each type of color filter, signals that are supposed to be obtained for the other types of color filter than the one provided for the pixels that are currently yielding image signals are produced by interpolating neighboring image signals. Then, by using the signals thus produced by interpolation and the image signals output from the CCD, color separation is performed, then primary color signals, i.e. R (red), G (green), and B (blue) signals are produced, then color difference signals R – Y and B – Y are produced, and eventually chrominance signals are produced

[0003] Fig.6 shows a conventional chrominance signal processing device that produces

chrominance signals from image signals output from a CCD as described above. In the chrominance signal processing device shown in Fig. 6, when image signals are fed in from a CCD, they are fed to a line memory 51 and to an adder circuit 53. The image signals output from the line memory 51 are fed to a line memory 52 and to a color separator circuit 55, and the image signals output from the line memory 52 are fed to the adder circuit 53. In this way, image signals from one row after another are stored in the line memory 51 and then in the line memory 52. The adder circuit 53 is fed with the image signals of the first row from the line memory 52 and the image signals of the third row directly from the CCD, and the image signals added together by the adder circuit 53 then have their signal levels multiplied by 1 / 2 by a multiplier circuit 54 so that the image signals of the first and third rows are averaged. Then, the image signals output from the multiplier circuit 54 and the image signals of the second row output from the line memory 51 are fed to the color separator circuit 55.

[0004] The color separator circuit 55 produces, for each image signal, three signals, namely a luminance signal YL and two color separation signals Cr and Cb, and feeds them to an RGB matrix circuit 56. From the luminance signal YL and the color separation signals Cr and Cb, the RGB matrix circuit 56 produces primary color signals, namely R, G, and B signals, from which a color difference matrix circuit 57 then produces color difference signals R – Y and B – Y. These color difference signals R – Y and B – Y are fed to a color encoder 58, which then produces and outputs chrominance signals.

[0005] The color separator circuit 55 is provided with color separation filters 59 and 60 for interpolating or correcting the image signals fed from the line memory 51 in the horizontal direction, color separation filters 61 and 62 for interpolating or correcting the image signals fed from the adder circuit 53 in the horizontal direction, an adder circuit 63 for adding

together the outputs from the color separation filters 59 and 60, a subtractor circuit 64 for calculating the difference between the outputs from the color separation filters 59 and 60, an adder circuit 65 for adding together the outputs from the color separation filters 61 and 62, a subtractor circuit 66 for calculating the difference between the outputs from the color separation filters 61 and 62, and an adder circuit 67 for adding together the outputs of the adder circuits 63 and 65.

[0006] Suppose that the chrominance signal processing device configured as described above is fed with image signals output from a CCD provided with four types of color filters, namely M (magenta), G (green), Y (yellow), and C (cyan) color filters, as shown at (a) in Fig. 3. As shown at (a) in Fig. 3, the CCD has two types of columns of color filters arranged alternately, specifically columns in which color filters are arranged in the order of M, Y, G, and Y and columns in which color filters are arranged in the order of G, C, M, and C. Moreover, the CCD outputs image signals obtained from two adjacent rows in combination. Specifically, as shown at (b) in Fig. 3, for every two rows, the CCD outputs image signals M + Y, G + C, G + Y, and M + C.

[0007] Let these image signals be expressed also as C1 = M + Y, C2 = G + C, C3 = G + Y, and C4 = M + C, respectively. Where image signals are output in this way, the colors M, C, and Y are expressed, in terms of primary colors R (red), G (green), and B (blue), as M = R + B, C = G + B, and Y = R + G, respectively. Hence, the image signals C1, C2, C3, and C4 are expressed, in terms of primary colors R, G, and B, as C1 = 2R + G + B, C2 = 2G + B, C3 = 2G + R, and C4 = 2B + G + R, respectively.

[0008] When image signals have been fed in in this way, for example, the chrominance

signals for pixels that yield the image signals C1 are produced in the following manner. First, the image signals C1 and C2 stored in the line memory 52 are fed to the color separation filters 59 and 60. Thus, the color separation filters 59 and 60 output the interpolated or corrected image signals C1 and C2. On the other hand, the image signals C3 and C4 fed directly from the CCD and the image signals C3 and C4 fed from the line memory 51 are averaged by the adder circuit 53 and the multiplier circuit 54, and are then fed to the color separation filters 61 and 62. Thus, the color separation filters 61 and 62 output the interpolated or corrected image signals C3 and C4.

[0009] When the image signals C2 to C4 for the pixels that yield the image signals C1 have been calculated plausibly in this way, the adder circuit 63 adds together the image signals C1 and C2, and the subtractor circuit 64 calculates the differences between the image signals C1 and C2. Simultaneously, the adder circuit 65 adds together the image signals C3 and C4, and the subtractor circuit 66 calculates the differences between the image signals C3 and C4. Then the outputs from the adder circuits 63 and 65 are added together by the adder circuit 67 to produce luminance signals YL, and the subtractor circuits 64 and 66 output color separation signals Cr and Cb, respectively. When the luminance signals YL and the color separation signals Cr and Cb have been produced in this way, the RGB matrix circuit 56 produces primary color signals, then the color difference matrix circuit 57 produces color difference signals, and then the color encoder 58 produces and outputs chrominance signals.

[0010] In the chrominance signal processing device shown in Fig. 6, the color separation filters 59 to 62 provided in the color separator circuit 55 thereof are each designed as a filter that performs calculation on three horizontally adjacent image signals, i.e. a target image signal and the image signals immediately preceding and succeeding it, with the color

separation filters 59 and 61 given filtering characteristics (0, 2, 0) and the color separation filters 60 and 62 given filtering characteristics (1, 0, 1).

[0011] Suppose that a color separation filter is given filtering characteristics (a, b, c), that the image signal from the pixel for which the chrominance signals are currently being calculated has a signal level "cb", and that the image signals output immediately before and after this image signal having the signal level "cb" have signal levels "ca" and "cc", respectively. Then, the color separation filter having these filtering characteristics produces and outputs an image signal having a signal level "a × ca + b × cb + c × cc". In the filtering characteristics (a, b, c) of a color separation filter, the components, here "a", "b", and "c", are called "taps", of which the number represents the number of image signals that the color separation filter uses to produce a signal.

[0012] Thus, with the color filters 59 to 62 having the filtering characteristics (0, 2, 0) and (1, 0, 1) as described above, for example, when image signals C1 and C2 of which the signal levels vary as shown in Fig. 7A are fed to the color separation filters 59 and 60, they are output with their signal levels interpolated as shown in Figs. 7B and 7C. Accordingly, when an edge is encountered at a position A between the fourth and fifth columns of pixels as shown in Fig. 7A, the image signals C1 and C2 immediately preceding and succeeding the position A are averaged and thereby interpolated by the image signals C1 and C2 preceding and succeeding them.

[0013] The image signals C1 and C2 thus interpolated and output from the color separation filters 59 and 60 are fed to the subtractor circuit 64, which then subtracts the image signals C1 from the image signals C2 and thereby produces color separation signals Cr.

Here, whereas ideally the signal levels of the color separation signals Cr should remain 0 all the time as shown in Figs. 7E, 7F, and 7G, in reality they become greater than 0 around the edge encountered at the position A as shown in Figs. 7B, 7C, and 7D, and thus contain certain non-zero components. This causes the edge to appear falsely colored.

[0014] On the other hand, with the color separation filters 59 to 62 given a larger number of taps, when image signals C1 and C2 as shown in Fig. 7A are fed thereto, they are interpolated and output as shown in Figs. 7H and 7I. Here, the levels of the image signals C1 and C2 that are actually output are themselves corrected by the image signals preceding and succeeding them. Thus, the levels of the image signals C1 and C2 that are actually output themselves vary, and as a result the signal levels of the color separation signals Cr are closer to the ideal value around the edge as shown in Fig. 7J than is shown in Fig. 7D. This helps alleviate the false coloring of the edge. However, the color separation signals thus obtained have signal levels deviated from the ideal value on the whole, and thus the portion of the image corresponding thereto is falsely colored on the whole.

[0015] As described above, in interpolating image signals in the horizontal direction, using color separation filters with a small number of taps causes the signal levels of the color separation signals to deviate greatly from the ideal value around an edge, and using color separation filters with a large number of taps causes the signal levels of the color separation signals to deviate from the ideal value on the whole. Thus, in either case, false coloring occurs.

[0016] On the other hand, in the vertical direction, the image signals fed directly from the CCD and the image signals fed from the line memory 52 are averaged and thereby linearly

interpolated by the adder circuit 53 and the multiplier circuit 54. As a result, when the subtractor circuit 64 outputs color separation signals Cr, the subtractor circuit 66 outputs linearly interpolated color separation signals Cb. Now, suppose that, as shown in Fig.8A, an edge is encountered at a position B between the second and third rows. Then, the subtractor circuit 64 outputs color separation signals Cr for the first and third rows and color separation signals Cb for the second and fourth rows, respectively having signal levels as shown in Figs. 8B and 8C.

[0017] Here, as shown in Figs. 8D and 8E, the signal level of the color separation signal Cr of the second row output from the subtractor circuit 66 is equal to the value obtained by linearly interpolating the signal levels of the color separation signals Cr of the first and third rows, and the signal level of the color separation signal Cb of the third row output from the subtractor circuit 66 is equal to the value obtained by linearly interpolating the signal levels of the color separation signals Cb of the second and fourth rows. Since an edge is encountered at the position B now, the ideal values of the signal levels of the color separation signals Cr and Cb are as shown in Figs. 8F and 8G. As will be clear from comparison between what is shown in Figs. 8D and 8E and what is shown in Figs. 8F and 8G, the color separation signal Cr of the second row and the color separation signal Cb of the third row have signal levels either lower or higher than their ideal values. Thus, when linear interpolation is performed in this way, false coloring occurs in the vertical direction also.

SUMMARY OF THE INVENTION

[0018] An object of the present invention is to provide a color separator circuit and a chrominance signal processing device that alleviate false coloring when image signals for a plurality of types of color filters are obtained by interpolation and chrominance signals are

produced from such image signals.

[0019] To achieve the above object, according to one aspect of the present invention, a color separator circuit for performing color separation on image signals fed thereto from a solid-state image-sensing device having pixels provided with a plurality of types of color filters is provided with: a contour detector for detecting the contour of a subject sensed by the solid-state image-sensing device by recognizing variations in the signals levels of the image signals fed from the solid-state image-sensing device; a first color separation filter for correcting the image signals fed from the solid-state image-sensing device by correcting each image signal based on a plurality of preceding and succeeding image signals; a second color separation filter for correcting the image signals fed from the solid-state image-sensing device by correcting each image signal based on a plurality of preceding and succeeding image signals; and a selector for selecting the second color separation filter when correcting image signals that represent a portion of an image that corresponds to the contour detected by the contour detector and selecting the first color separation filter when correcting image signals that represent a portion of the image other than the portion corresponding to the contour. Here, the first color separation filter uses a smaller number of image signals to correct an image signal than the second color separation filter.

[0020] According to another aspect of the present invention, in a chrominance signal processing device that produces chrominance signals based on signals output from a color separator circuit provided therein, the color separator circuit is provided with: a contour detector for detecting the contour of a subject sensed by a solid-state image-sensing device having pixels provided with a plurality of types of color filters by recognizing variations in the signals levels of image signals fed from the solid-state image-sensing device to the

contour detector; a first color separation filter for correcting the image signals fed from the solid-state image-sensing device by correcting each image signal based on a plurality of preceding and succeeding image signals; a second color separation filter for correcting image signals fed from the solid-state image-sensing device by correcting each image signal based on a plurality of preceding and succeeding image signals; and a selector for selecting the second color separation filter when correcting image signals that represent a portion of an image that corresponds to the contour detected by the contour detector and selecting the first color separation filter when correcting image signals that represent a portion of the image other than the portion corresponding to the contour. Here, the first color separation filter uses a smaller number of image signals to correct an image signal than the second color separation filter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] This and other objects and features of the present invention will become clear from the following description, taken in conjunction with the preferred embodiments with reference to the accompanying drawings in which:

Fig. 1 is a block diagram showing the internal configuration of a chrominance signal processing device embodying the invention;

Fig. 2 is a block diagram showing the internal configuration of the color separator circuit provided in the chrominance signal processing device shown in Fig. 1;

Fig. 3 is a diagram showing the relationship between the color filters provided one for each of the pixels of the CCD and the image signals output from the CCD;

Figs. 4A to 4M are diagrams showing how signals are processed by the color separator circuit shown in Fig. 2;

Figs. 5A to 5F are diagrams showing how signals are processed by the color separator circuit shown in Fig. 2;

Fig. 6 is a block diagram showing the internal configuration of a conventional chrominance signal processing device;

Figs. 7A to 7J are diagrams showing how signals are processed by the color separator circuit provided in the chrominance signal processing device shown in Fig. 6; and

Figs. 8A to 8G are diagrams showing how signals are processed by the color separator circuit provided in the chrominance signal processing device shown in Fig. 6.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022] Hereinafter, an embodiment of the present invention will be described with reference to the drawings. Fig. 1 is a block diagram showing the internal configuration of the chrominance signal processing device of the embodiment. Fig. 2 is a block diagram showing the internal configuration of the color separator circuit provided in the chrominance signal processing device shown in Fig. 1.

Configuration and Operation of the Chrominance Signal Processing Device

[0023] The chrominance signal processing device shown in Fig. 1 is provided with a line memory 1 for storing image signals output from a CCD, a line memory 2 for storing the image signals output from the line memory 1, a color separator circuit 3 that is fed with image signals constituting three vertically adjacent rows from the CCD and from the line memories 1 and 2, an RGB matrix circuit 4 for producing primary color signals, i.e. R, G, and B signals, from the luminance signals YL and the color separation signals Cr and Cb output from the color separation circuit 3, a color difference matrix circuit 5 for producing color difference signals R – Y and B – Y from the primary color signals R, G, and B output from the RGB

matrix circuit 4, and a color encoder 6 for producing chrominance signals from the color difference signals R – Y and B – Y output from the color difference matrix circuit 5.

[0024] In this chrominance signal processing device configured as described above, when image signals are received from the CCD, they are fed to the line memory 1 and to the color separator circuit 3. In the line memory 1 are stored horizontally adjacent image signals that together constitute a row. The image signals output from the line memory 1 are fed to the line memory 2 and to the color separator circuit 3, so that horizontally adjacent image signals that together constitute a row are stored in the line memory 2 also. The image signals output from the line memory 2 are, like those output from the line memory 1, fed to the color separator circuit 3. In this way, the color separator circuit 3 is fed with the image signals of a first row from the line memory 2, the image signals of a second row from the line memory 1, and the image signals of a third row from the CCD, and thus receives image signals constituting three vertically adjacent rows.

[0025] Now, suppose that, as described previously, the CCD has color filters M, G, C, and Y arranged as shown at (a) in Fig. 3 and outputs image signals C1 to C4 as shown at (b) in Fig. 3. Then, the color separator circuit 3, on the basis of the plurality of image signals fed thereto from the CCD and from the line memories 1 and 2, produces a luminance signal YL and color separation signals Cr and Cb for each of those image signals. As a luminance signal YL and color separation signals Cr and Cb are produced for each image signal, the RGB matrix circuit 4, on the basis of the thus produced signals, produces primary color signals R, G, and B.

[0026] Then, on the basis of these primary color signals R, G, and B, the color difference

matrix circuit 5 produces color difference signals R – Y and B – Y (where R – Y = 0.70R – 0.59G – 0.11B and B – Y = –0.30R – 0.59G + 0.89B). These color difference signals R – Y and B – Y are fed to the color encoder 6, which then forms those signals into signals having a phase difference of 90° relative to each other and then mixes them together to produce and output chrominance signals. In this chrominance signal processing device, the color separator circuit 3 is configured and operates as described below.

Configuration of the Color Separator Circuit

[0027] As shown in Fig. 2, the color separator circuit 3 is provided with an edge detection filter 7a and color separation filters 8a, 9a, 10a, and 11a that are fed with image signals from the CCD, an edge detection filter 7b and color separation filters 8b, 9b, 10b, and 11b that are fed with image signals from the line memory 1, and an edge detection filter 7c and color separation filters 8c, 9c, 10c, and 11c that are fed with image signals from the line memory 2. Of these color separation filters, the color separation filters 8a, 10a, 8b, 10b, 8c, and 10c are small-tap-number filters having a small number of taps, and the color separation filters 9a, 11a, 9b, 11b, 9c, and 11c are large-tap-number filters having a large number of taps

[0028] The color separator circuit 3 is further provided with a selector circuit 12a consisting of a switch SW1a for choosing between the image signals from the color separation filters 8a and 9a and a switch SW2a for choosing between the image signals from the color separation filters 10a and 11a, a selector circuit 12b consisting of a switch SW1b for choosing between the image signals from the color separation filters 8b and 9b and a switch SW2b for choosing between the image signals from the color separation filters 10b and 11b, and a selector circuit 12c consisting of a switch SW1c for choosing between the image signals from the color separation filters 8c and 9c and a switch SW2c for choosing between the image

signals from the color separation filters 10c and 11c. This makes it possible to choose between the image signals obtained from the small-tap-number filters and those obtained from the large-tap-number filters. The selecting operation of the selector circuits 12a, 12b, and 12c is controlled according to the signals fed individually thereto from the edge detection filters 7a to 7c.

[0029] Two image signals chosen by the selector circuit 12a are added together by an adder circuit 13a, and their difference is calculated by a subtractor circuit 14a, two image signals chosen by the selector circuit 12b are added together by an adder circuit 13b, and their difference is calculated by a subtractor circuit 14b, and two image signals chosen by the selector circuit 12c are added together by an adder circuit 13c, and their difference is calculated by a subtractor circuit 14c. Then, the outputs of the adder circuits 13a, 13b, and 13c are fed to a vertical-direction low-pass filter (hereinafter abbreviated to "VLPF") 15 and to a ratio calculator circuit 16. The outputs of the subtractor circuits 14a and 14c are added together by an adder circuit 17, and then the result is multiplied, by a multiplier circuit 18, by the ratio calculated by the ratio calculator circuit 16. As a result, the VLPF 15 outputs a luminance signal YL, one of the subtractor circuit 14b and the multiplier circuit 18 outputs a color separation signal Cr, and the other of the subtractor circuit 14b and the multiplier circuit 18 outputs a color separation signal Cb.

[0030] The operation of the color separator circuit 3 configured as described above will be described below, in particular from the perspective of how it achieves reduction of false coloring that occurs both in the horizontal and vertical directions.

How False Coloring in the Horizontal Direction is Reduced

[0031] Reduction of false coloring in the horizontal direction is performed by the edge detection filters 7a to 7c, the color separation filters 8a to 8c, 9a to 9c, 10a to 10c, and 11a to 11c, and the selector circuits 12a to 12c. Here, it is assumed that the color separation filters 8a to 8c have filtering characteristics (0, x1, 0) and the color separation filters 10a to 10c have filtering characteristics (x2, 0, x3), where x1 to x3 are values that fulfill the relation x1 = x2 + x3. Moreover, it is assumed that the color separation filters 9a to 9c have filtering characteristics (0, y1, 0, y2, 0, y3, 0) and the color separation filters 10a to 10c have filtering characteristics (y4, 0, y5, 0, y6, 0, y7), where y1 to y7 are values that fulfill the relation y1 + y2 + y3 = y4 + y5 + y6 +y7.

[0032] The edge detection filters 7a to 7c, the color separation filters 8a to 8c, 9a to 9c, 10a to 10c, and 11a to 11c, and the selector circuits 12a to 12c operate in the same manner, and therefore the following descriptions deal with, as their representatives, only the operation of the edge detection filter 7a, the color separation filters 8a, 9a, 10a, and 11a, and the selector circuit 12a.

[0033] Suppose that image signals Cx and Cy including an edge at a position A between the fourth and fifth columns as shown in Fig. 4A, like those shown in Fig. 7A, are fed to the edge detection filter 7a and to the color separation filters 8a to 11a. Here, it is assumed that the image signals Cx and Cy of the first to fourth columns all have a signal level "ca" and the image signals Cx and Cy of the fifth to eighth columns all have a signal level "cb". Moreover, it is assumed that the image signals preceding the first column have a signal level "ca" and the image signals succeeding the eighth column have a signal level "cb". Moreover, if it is assumed that the image signals Cx are image signals C1, C2, C3, and C4, then the

image signals Cy are image signals C2, C1, C4, and C3.

1. Edge Detection Filters

[0034] First, the edge detection filter 7a detects the edge at the position A in the image signals Cx and Cy, which are fed in alternately, and feeds a control signal to the selector circuit 12a. Here, the edge detection filter 7a is given filtering characteristics (–1, 2, –1) to make it possible to extract the edge from the image signals, which are fed in continuously. Specifically, when the edge detection filter 7a receives three image signals that have signal levels c1, c2, and c3, respectively, it performs calculation $c1 \times (-1) + c2 \times 2 + c3 \times (-1)$. Thus, when the edge detection filter 7a receives image signals Cx and Cy of which the signal levels vary as shown in Fig. 4A, it yields calculation results as shown in Fig. 4B.

[0035] Specifically, the calculation results are $ca \times (-1) + ca \times 2 + ca \times (-1) = 0$ for the first to third columns, $ca \times (-1) + ca \times 2 + cb \times (-1) = ca - cb$ for the fourth column, $ca \times (-1) + cb \times 2 + cb \times (-1) = cb - ca$ for the fifth column, and $cb \times (-1) + cb \times 2 + cb \times (-1) = 0$ for the sixth to eighth columns. In this way, the calculation results are non-zero at the edge encountered at the position A. Each of the results E1 of the calculation performed by the edge detection filter 7a is checked to determine whether $-Th \leq E1 \leq Th$ or not, and, if $E1 < -Th$ or $E1 > Th$, an edge is recognized to exist. In the case of the example shown in Figs. 4A to 4M, if it is assumed that $ca - cb > Th$, an edge is recognized to exist in the fourth and fifth columns.

2. Small-tap-number Color Separation Filters

[0036] When the color separation filter 8a receives three image signals having signal levels c1, c2, and c3, respectively, it performs calculation $c1 \times 0 + c2 \times x1 + c3 \times 0 = c2 \times x1$.

When the color separation filter 10a receives, as the color separation filter 8a does, three image signals having signal levels c1, c2, and c3, respectively, it performs calculation $c1 \times x2 + c2 \times 0 + c3 \times x3 = c1 \times x2 + c3 \times x3$. Thus, when the color separation filters 8a and 10a receive image signals Cx and Cy of which the signal levels vary as shown in Fig. 4A, they yield calculation results as shown in Figs. 4C and 4D.

[0037] Specifically, the color separation filter 8a outputs image signals Cx and Cy having a signal level $ca \times x1$ for the first to fourth columns and image signals Cx and Cy having a signal level $cb \times x1$ for the fifth to eighth columns. On the other hand, the color separation filter 10a outputs image signals Cx and Cy having a signal level $ca \times (x2 + x3) = ca \times x1$ for the first to third columns, an image signal Cx having a signal level $ca \times x2 + cb \times x3$ for the fourth column, an image signal Cy having a signal level $ca \times x2 + cb \times x3$ for the fifth column, and image signals Cx and Cy having a signal level $cb \times (x2 + x3) = cb \times x1$ for the sixth to eighth columns.

[0038] As a result, the image signals Cx and Cy fed to the selector circuit 12a have signal levels as shown in Figs. 4E and 4F. Specifically, for the first to third columns, the image signals Cx and Cy both have a signal level $ca \times x1$, and, for the sixth to eighth columns, the image signals Cx and Cy both have a signal level $cb \times x1$. For the fourth column, the image signal Cx has a signal level $ca \times x2 + cb \times x3$ and the image signal Cy has a signal level $ca \times x1$. For the fifth column, the image signal Cx has a signal level $ca \times x1$ and the image signal Cy has a signal level $ca \times x2 + cb \times x3$.

3. Large-tap-number Color Separation Filters

[0039] When the color separation filter 9a receives seven image signals having signal levels c1, c2, c3, c4, c5, c6, and c7, respectively, it performs calculation $c1 \times 0 + c2 \times y1 + c3 \times 0 + c4 \times y2 + c5 \times 0 + c6 \times y3 + c7 \times 0 = c2 \times y1 + c4 \times y2 + c6 \times y3$. When the color separation filter 11a receives, as the color separation filter 9a does, seven image signals having signal levels c1, c2, c3, c4, c5, c6, and c7, respectively, it performs calculation $c1 \times y4 + c2 \times 0 + c3 \times y5 + c4 \times 0 + c5 \times y6 + c6 \times 0 + c7 \times y7 = c1 \times y4 + c3 \times y5 + c5 \times y6 + c7 \times y7$. Thus, when the color separation filters 9a and 11a receive image signals Cx and Cy of which the signal levels vary as shown in Fig. 4A, they yield calculation results as shown in Figs. 4G and 4H.

[0040] Specifically, the color separation filter 9a outputs image signals Cx and Cy having a signal level $ca \times (y1 + y2 + y3)$ for the first and second columns, image signals Cx and Cy having signal levels $ca \times (y1 + y2) + cb \times y3$ for the third and fourth columns, image signals Cx and Cy having signal levels $ca \times y1 + cb \times (y2 + y3)$ for the fifth and sixth columns, and image signals Cx and Cy having signal levels $cb \times (y1 + y2 + y3)$. On the other hand, the color separation filter 11a outputs an image signal Cy having a signal level $ca \times (y4 + y5 + y6 + y7) = ca \times (y1 + y2 + y3)$ for the first column, image signals Cx and Cy having a signal level $ca \times (y4 + y5 + y6) + cb \times y7$ for the second and third columns, image signals Cx and Cy having a signal level $ca \times (y4 + y5) + cb \times (y6 + y7)$ for the fourth and fifth columns, image signals Cx and Cy having a signal level $ca \times y4 + cb \times (y5 + y6 + y7)$ for the sixth and seventh columns, and an image signal Cx having a signal level $cb \times (y4 + y5 + y6 + y7) = cb \times (y1 + y2 + y3)$.

[0041] As a result, the image signals Cx and Cy fed to the selector circuit 12a have signal levels as shown in Figs. 4I and 4J. Specifically, for the first column, the image signals Cx and Cy both have a signal level ca × (y1 + y2 + y3), and, for the eighth column, the image signals Cx and Cy both have a signal level cb × (y1 + y2 + y3). For the second column, the image signal Cx has a signal level ca × (y4 + y5 + y6) + cb × y7 and the image signal Cy has a signal level ca × (y1 + y2 + y3). For the third column, the image signal Cx has a signal level ca × (y1 + y2) + cb × y3 and the image signal Cy has a signal level ca × (y4 + y5 + y6) + cb × y7.

[0042] For the fourth column, the image signal Cx has a signal level ca × (y4 + y5) + cb × (y6 + y7) and the image signal Cy has a signal level ca × (y1 + y2) + cb × y3. For the fifth column, the image signal Cx has a signal level ca × y1 + cb × (y2 + y3) and the image signal Cy has a signal level ca × (y4 + y5) + cb × (y6 + y7). For the sixth column, the image signal Cx has a signal level ca × y4 + cb × (y5 + y6 + y7) and the image signal Cy has a signal level ca × y1 + cb × (y2 + y3). For the seventh column, the image signal Cx has a signal level cb × (y1 + y2 + y3) and the image signal Cy has a signal level ca × y4 + cb × (y5 + y6 + y7).

4. Selector Circuits

[0043] In the selector circuit 12a, according to the control signal fed thereto from the edge detection filter 7a, either the outputs of the small-tap-number color separation filters 8a and 10a or the outputs of the large-tap-number color separation filters 9a and 11a are chosen and fed to the adder circuit 13a and to the subtractor circuit 14a. Here, the selector circuit 12a is controlled by the control signal fed thereto from the edge detection filter 7a in such a way that the large-tap-number color separation filters 9a and 11a are chosen when an edge is

encountered. Specifically, when the result E1 of the calculation performed by the edge detection filter 7a fulfills $-Th \leq E1 \leq Th$, the terminals "a" of the switches SW1a and SW2a are connected to their respective common terminals so that the outputs of the small-tap-number color separation filters 8a and 10a are chosen; by contrast, when the result E1 of the calculation performed by the edge detection filter 7a fulfills $E1 \leq -Th$ or $E1 \geq Th$, the terminals "b" of the switches SW1a and SW2a are connected to their respective common terminals so that the outputs of the large-tap-number color separation filters 9a and 11a are chosen.

[0044] Thus, when the edge detection filter 7a yields calculation results as shown in Fig. 4B, for the first to third and sixth to eighth columns, the image signals Cx and Cy, as shown in Figs. 4E and 4F, output from the small-tap-number color separation filters 8a and 10a are chosen, and, for the fourth and fifth columns, the image signals Cx and Cy, as shown in Figs.4I and 4J, output from the large-tap-number color separation filters 9a and 11a are chosen.

[0045] As a result, the selector circuit 12a feeds image signals Cx and Cy as shown in Figs. 4K and 4L to the adder circuit 13a and to the subtractor circuit 14a. Specifically, for the first to third columns, the image signals Cx and Cy both have a signal level $ca \times x1$, and, for the sixth to eighth columns, the image signals Cx and Cy both have a signal level $cb \times x1$. For the fourth column, the image signal Cx has a signal level $ca \times (y4 + y5) + cb \times (y6 + y7)$ and the image signal Cy has a signal level $ca \times (y1 + y2) + cb \times y3$. For the fifth column, the image signal Cx has a signal level $ca \times y1 + cb \times (y2 + y3)$ and the image signal Cy has a signal level $ca \times (y4 + y5) + cb \times (y6 + y7)$.

[0046] As the selector circuit 12a outputs image signals Cx and Cy in this way, when the image signals Cx are image signals C1 and C2, the adder circuit 13a outputs a luminance signal YLa that is equal to C1 + C2 and the subtractor circuit 14a outputs a color separation signal Cra that is equal to C2 – C1; when the image signals Cx are image signals C3 and C4, the adder circuit 13a outputs a luminance signal YLa that is equal to C3 + C4 and the subtractor circuit 14a outputs a color separation signal Cba that is equal to C4 – C3.

[0047] Thus, when the selector circuit 12a outputs image signals Cx and Cy as shown in Figs. 4K and 4L, the subtractor circuit 14a outputs signals as shown in Fig. 4M. Specifically, the color separation signals Cra or Crb have a signal level 0 for the first to third and sixth to eighth columns, a signal level $|\,[ca \times (y4 + y5) + cb \times (y6 + y7)] - [ca \times (y1 + y2) + cb \times y3]\,|$ for the fourth column, and a signal level $|\,(ca \times y1 + cb \times (y2 + y3)) - [ca \times (y4 + y5) + cb \times (y6 + y7)]\,|$.

[0048] The edge detection filters 7b and 7c, the color separation filters 8b, 8c, 9b, 9c, 10b, 10c, 11b, and 11c, and the selector circuits 12b and 12c operate in the same manner as the edge detection filter 7a, the color separation filters 8a., 9a, 10a, and 11a, and the selector circuit 12a described above. When the selector circuits 12b and 12c output image signals C1 and C2, the adder circuits 13b and 13c output luminance signals YLb and YLc, respectively, each having a signal level C1 + C2, and the subtractor circuits 14b and 14c output color separation signals Crb and Crc, respectively, each having a signal level C1 – C1. By contrast, when the selector circuits 12b and 12c output image signals C3 and C4, the adder circuits 13b and 13c output luminance signals YLb and YLc, respectively, each having a signal level C3 + C4, and the subtractor circuits 14b and 14c output color separation signals Cbb and Cbc, respectively, each having a signal level C4 – C3.

[0049] In this way, by using, where an edge is encountered, the outputs of the large-tap-number color separation filters, which deviate only slightly from the ideal values, and using, where no edge is encountered, the outputs of the small-tap-number color separation filters, which are almost equal to the ideal values, it is possible to make the signal levels of the color separation signals Cr and Cb closer to their ideal values and thereby reduce false coloring in the horizontal direction. It is to be understood that the color separation filters may have any number of taps other than three and seven specifically described above, as long as the large-tap-number color separation filters have a larger number of taps than the small-tap-number color separation filters.

How False Coloring in the Horizontal Direction is Reduced

[0050] Reduction of false coloring in the vertical direction is performed by the VLPF 15, the ratio calculator circuit 16, the adder circuit 17, and the multiplier circuit 18. The luminance signals YLa, YLb, and YLc output from the adder circuits 13a, 13b, and 13c as described above are fed to the VLPF 15 and to the ratio calculator circuit 16. Here, when the luminance signal YLa is a signal that is equal to C1 + C2, the luminance signal YLb is a signal that is equal to C3 + C4, and the luminance signal YLc is a signal that is equal to C1 + C2. By contrast, when the luminance signal YLa is a signal that is equal to C3 + C4, the luminance signal YLb is a signal that is equal to C1 + C2, and the luminance signal YLc is a signal that is equal to C3 + C4.

[0051] When the adder circuit 13a outputs a luminance signal YLa that is equal to C1 + C2, the subtractor circuits 14a and 14c output color separation signals Cra and Crc, respectively, and the subtractor circuit 14b outputs a color separation signal Cbb. By contrast, when the adder circuit 13a outputs a luminance signal YLa that is equal to C3 + C4,

the subtractor circuits 14a and 14c output color separation signals Cba and Cbc, respectively, and the subtractor circuit 14b outputs a color separation signal Crb.

[0052] From the luminance signals YLa, YLb, and YLc, the VLPF 15 produces a luminance signal YL and outputs it. This luminance signal YL is produced by performing calculation $YL = 2 \times (1 - \alpha)\, YLb + \alpha\, (YLa + YLc)$, where α fulfills the relation $0 < \alpha < 1$. The luminance signal YL thus produced is, as described previously, fed to the RGB matrix circuit 4. On the other hand, from the luminance signals YLa, YLb, and YLc, the ratio calculator circuit 16 produces a ratio β to be fed to the multiplier circuit 18 to multiply therewith the signal output from the adder circuit 17. If it is assumed that the luminance signals YLa, YLb, and YLc have signal levels yLa, yLb, and yLc, then the ratio β is produced by performing calculation $\beta = yLb / (yLa + yLc)$.

[0053] Now, with reference to Figs. 5A to 5F, the color separation signals Cr and Cb, which are fed to the RGB matrix circuit together with the luminance signal YL, will be described. Suppose that an edge is encountered at a position B between the second and third rows as shown in Fig. 5A in the same manner as shown in Fig. 8A. Here, it is assumed that the subtractor circuits 14a, 14b, and 14c produce color separation signals Cz from the image signals of the first and third rows and color separation signals Cw from the image signals of the second and fourth rows. It is to be noted that, when the color separation signals Cz are color separation signals Cr, the color separation signals Cw are color separation signals Cb and, when the color separation signals Cz are color separation signals Cb, the color separation signals Cw are color separation signals Cr.

[0054] As image signals including an edge as shown in Fig. 5A are fed to the color

separator circuit 3, as shown in Figs. 5B, 5C, and 5D, when the image signal of the first or third row is fed in from the line memory 1, the subtractor circuit 14b outputs an image color separation signal Cz and, when the image signal of the second or fourth row is fed in from the line memory 1, the subtractor circuit 14b outputs an image color separation signal Cw.

[0055] When the color separator circuit 3 is fed with the image signal of the first row shown in Fig. 5A from the line memory 2, the image signal of the second row shown in Fig. 5A from the line memory 1, and the image signal of the third row shown in Fig. 5A from the CCD, the adder circuit 17 and the multiplier circuit 18 operate in the following manner. This time, the subtractor circuits 14a and 14c output color separation signals Cz and the subtractor circuit 14b outputs a color separation signal Cw. Here, let the color separation signals Cz output from the subtractor circuit 14a be color separation signals Cza and the color separation signals Cz output from the subtractor circuit 14c be color separation signals Czb.

[0056] Then, if it is assumed that the color separation signals Cza and Czb have signal levels cza and czb, the adder circuit 17 adds together the color separation signals Cza and Czb output from the subtractor circuits 14a and 14c, and feeds the resulting signal cza + czb to the multiplier circuit 18. When the signals fed from the adder circuits 13a, 13b, and 13c to the VLPF 15 have signal levels Ya, Ya, and Yb as shown in Figs. 5B, 5C, and 5D, the ratio calculator circuit 16 feeds a ratio β that is equal to Ya / (Ya + Yb) to the multiplier circuit 18. As a result, as shown in Fig. 5E, the multiplier circuit 18 outputs a color separation signal Cz that is equal to $(cza + czb) \times Ya / (Ya + Yb)$.

[0057] Similarly, when the color separator circuit 3 is fed with the image signal of the second row shown in Fig. 5A from the line memory 2, the image signal of the third row

shown in Fig. 5A from the line memory 1, and the image signal of the fourth row shown in Fig. 5A from the CCD, the adder circuit 17 and the multiplier circuit 18 operate in the following manner. This time, the subtractor circuits 14a and 14c output color separation signals Cw and the subtractor circuit 14b outputs a color separation signal Cz. Here, let the color separation signals Cw output from the subtractor circuit 14a be color separation signals Cwa and the color separation signals Cw output from the subtractor circuit 14c be color separation signals Cwb.

[0058] Then, if it is assumed that the color separation signals Cwa and Cwb have signal levels cwa and cwb, the adder circuit 17 adds together the color separation signals Cwa and Cwb output from the subtractor circuits 14a and 14c, and feeds the resulting signal cwa + cwb to the multiplier circuit 18. When the signals fed from the adder circuits 13a, 13b, and 13c to the VLPF 15 have signal levels Ya, Yb, and Yb as shown in Figs. 5B, 5C, and 5D, the ratio calculator circuit 16 feeds a ratio β that is equal to Yb / (Ya + Yb) to the multiplier circuit 18. As a result, as shown in Fig. 5F, the multiplier circuit 18 outputs a color separation signal Cw that is equal to (cwa + cwb) $\times$ Yb / (Ya + Yb).

[0059] Moreover, if it is assumed that, of the signals fed to the VLPF 15, those corresponding to the image signals of the second and the preceding rows have a signal level Ya and those corresponding to the image signals of the third and the succeeding rows have a signal level Yb, the color separation signal Cw of the first row is made to have a signal level equal to that of the color separation signal Cw of the second row as shown in Fig. 5F as a result of the signal output from the adder circuit 17 being multiplied by a ratio β of 1 / 2 by the multiplier circuit 18. Similarly, the color separation signal Cz of the fourth row is made to have a signal level equal to that of the color separation signal Cz of the third row as shown

in Fig. 5E as a result of the signal output from the adder circuit 17 being multiplied by a ratio β of 1 / 2 by the multiplier circuit 18.

[0060] In this way, it is possible to make the signal levels of the color separation signals Cr and Cb closer to the level of the brightness of the light incident on the CCD and thereby reduce false coloring as compared with conventional methods whereby the signal levels of the color separation signals Cr and Cb are calculated by linear polarization.

Advantages of the Invention

[0061] As described above, according to the present invention, an edge is detected, and the image signals that correspond to the edge are processed by the use of large-tap-number color separation filters, which help reduce false coloring in the image signals corresponding to an edge as compared with small-tap-number color separation filters. On the other hand, the image signals other than those corresponding to an edge are processed by the use of small-tap-number color separation filters, which help reduce false coloring in the image signals other than those corresponding to an edge as compared with large-tap-number color separation filters. In this way, by switching color separation filters for processing image signals according to the brightness of the light incident on where image sensing is currently being performed, it is possible to reduce false coloring and thus perform color separation by interpolation in a manner closer to an ideal. Moreover, by performing interpolation of the color separation signals according to the ratio of the signal levels of the luminance signals, it is possible to make the color separation signals have signal levels closer to their ideal values and thereby reduce false coloring as compared with conventional methods whereby interpolation is achieved by linear interpolation.